PATENT CLAIMS

1. Scaleable integrated data processing device, particularly a microcomputer, comprising a processing unit, wherein the processing unit comprises one or more processors, and a storage unit, wherein the storage unit comprises one or more memories, and wherein the data processing device is provided on a carrier substrate (S),
characterized in
that the data processing device comprises mutually adjacent, substantially parallel stacked layers (P, M, MP),
that the processing unit and the storage unit are provided in one or more layers, the separate layers being provided with a selected number of processors and memories in selected combinations,
that each layer comprises in or on the layer horizontal electrical conducting structures which forms electrical internal connections in the layer, and
that each layer comprises further electrical structures which provide electrical connection to other layers and to the exterior of the data processing device.

2. Scaleable integrated data processing device according to claim 1, characterized in that one or more layers are realized in the form of a number of sublayers in a technology which on a first level of a functional hierarchy configures functionally one or more layers as a combined processor and memory layer (MP), or one or more layers substantially as processor layers (P) or one or more layers substantially as memory layers (M).

3. Scaleable integrated data processing device according to claim 2, characterized in that the processing unit in a layer (P, MP) is configured functionally on a second level of the functional hierarchy as one or more processors (5) or parts of one or more processors (5), at least one processor constituting a central processing unit or microprocessor (5) in the data processing device, and possible further processors optionally being configured as control and/or communication processors respectively.

4. Scaleable integrated data processing device according to claim 3, characterized in that the central processing (5) unit is configured functionally on a third level of the functional hierarchy as a parallel processor with several execution units working in parallel provided in one and the same

layer (P, MP) or in two or more layers (P, MP) or in sublayers of these layers to provide an optimal interconnection topology.

5. Scaleable integrated data processing device according to claim 2, wherein more than one central processing unit is provided, characterized in that each central processing unit (5) is mutually connected and adapted for working in parallel and provided in one and the same layer (P, MP) or in two or more layers (P, MP) to provide an optimal interconnection topology.

6. Scaleable integrated data processing device according to claim 3, characterized in that the storage unit in a layer (M, MP) is configured functionally on a second level of the functional hierarchy as one or more memories or parts of one or more memories, at least one memory constituting a RAM (6) and being connected with at least one central processing unit or microprocessor (5) in the data processing device, and possible further memories optionally being configured as high-speed memories, ROMs, WORM, ERASABLE and REWRITEABLE respectively.

7. Scaleable integrated data processing device according to claim 6, characterized in that two or more RAMs (6) are connected to a central processing unit and respectively assigned to two or more subunits in the central processing unit (5), RAMs (6) and subunits being distributed in selected combinations in one or more layers (P, M, MP) to provide an optimal interconnection topology.

8. Scaleable integrated data processing device according to claim 6, wherein two or more central processing units (5) which are connected with one or more common RAM or RAMs (6), characterized in that each central processing unit is provided in mutually adjacent layers (P, MP), or distributed in selected combinations between two or more layers (P, MP), and that the common RAM or RAMs are provided in selected combinations in one or more of the central processing layers (P, MP) and/or in one or more memory layers (M) adjacent to the central processing layers or interfoliated therebetween to provide an optimal interconnection topology.

9. Scaleable integrated data processing device according to claim 6, characterized in that at least a part of the storage unit constitutes a mass

memory, the mass memory optionally being configured as RAM, ROM, WORM or ERASABLE or REWRITEABLE or combinations thereof.

10. Scaleable integrated data processing device according to claim 2, wherein the data processing unit comprises several processor layers (P) and several memory layers (M), characterized in that the memory layers (M) in order to reduce the signal paths therebetween and the processor layers (P) are interfoliated between the latter.

11. Scaleable integrated data processing device according to claim 1, characterized in that further electrical structures in a layer (P, M, MP) are provided on at least a side edge of the layer as an electrical edge connection.

12. Scaleable integrated data processing device according to claim 1, characterized in that the further electrical conducting structures in a layer (P, M, MP) are provided as vertical conducting structures which form an electrical connection in the cross direction of the layer and perpendicular to its plane to contact electrical conducting structures in other layers.

13. Scaleable integrated data processing device according to claim 1, characterized in that one or more layers (P, M, MP) are formed of an organic thin-film material, the organic thin-film material or materials being selected among monomers, oligomers and polymeric organic materials and metal organic complexes, or combinations of materials of this kind.

14. Scaleable integrated data processing device according to claim 13, characterized in that all layers (P, M, MP) are formed of organic thin-film material.

15. Scaleable integrated data processing device according to claim 1, characterized in that one or more layers (P, M, MP) are formed of inorganic thin-film material, the inorganic thin-film material or materials being selected among crystalline, polycrystalline and amorphous thin-film materials, or combinations of materials of this kind.

16. Scaleable integrated data processing device according to claim 13~~or 14~~, characterized in that two or more layers (P, M, MP) are formed of both organic and inorganic thin-film materials or combinations of materials of this kind.